

DIGITAL WAVEGUIDES VS. WAVE DIGITAL FILTERS IN PHYSICAL MODELING: THEORETICAL AND COMPUTATIONAL ASPECTS

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ABSTRACT

Digital Waveguides (DWG) are known as a highly efficient approach to physical modeling and sound synthesis of musical instruments. Recently there has been increasing interest in studying other discrete-time paradigms such as Finite Difference Time Domain (FDTD) schemes as well as Wave Digital Filters (WDF) and their combinations for the same task domain. In this paper we investigate the relation of DWGs and WDFs from new viewpoints. DSP techniques for efficient computation of the models are studied with particular interest in block-based (object-based) formulation for mixed paradigm physical modeling.

1. INTRODUCTION

Physical modeling of musical instruments and physics-based sound synthesis has been an active field of research, where particularly the principles of *Digital Waveguides* (DWG) [1] and *networks* (DWN) [2] have become popular. DWGs allow for efficient and easy implementation of delay-lines by DSP in order to simulate traveling wave propagation in substructures of musical instruments.

Another principle of physical modeling that is used especially in multidimensional mesh-like structures is the *Finite Difference Time Domain* (FDTD) [3] simulation of spatially distributed systems. We have recently shown the fundamental similarity between DWGs and FDTD structures [4].

The third physical modeling principle, well-known in digital simulation of analog circuits, is the *Wave Digital Filters* (WDF) [5]. There has been increasing interest in investigating relations between the DWG, FDTD, and WDF paradigms for physical modeling [6] as well as developing mixed modeling paradigms to combine these methods within a single model [7, 8, 4].

In this paper we discuss the relation between digital waveguides and wave digital filters from a new point of view. By an extended analysis of DWG structures and network topologies we end up with different ways to realize lumped element admittances, one of them being equivalent to the WDF formulation. Another variant is based on Kirchhoff variables instead of wave variables, and is therefore called here the Kirchhoff Digital Filter (KDF) approach.

2. DIGITAL WAVEGUIDE STRUCTURES

The idea of *Digital Waveguides* [1] starts from modeling of wave propagation by using digital delay-lines. In a one-dimensional medium the basic form of the wave equation is written $y_{tt} = c^2 y_{xx}$ where y is a physical variable, subscript tt refers to the second partial derivative in time t , xx to the second partial derivative in spatial variable x , and c is speed of wavefront in the medium of interest. Digital Waveguides (DWGs) are based on the d'Alembert's solution of the wave equation as two traveling wave components propagating in opposite directions. Digital simulation of an ideal lossless medium is simple: wave propagation is represented by two delay lines, one shifting a wave to the left and the other one shifting another wave to the right as

$$\vec{y}_{k,n+1} = \vec{y}_{k-1,n} \quad \text{and} \quad \overleftarrow{y}_{k,n+1} = \overleftarrow{y}_{k+1,n}$$

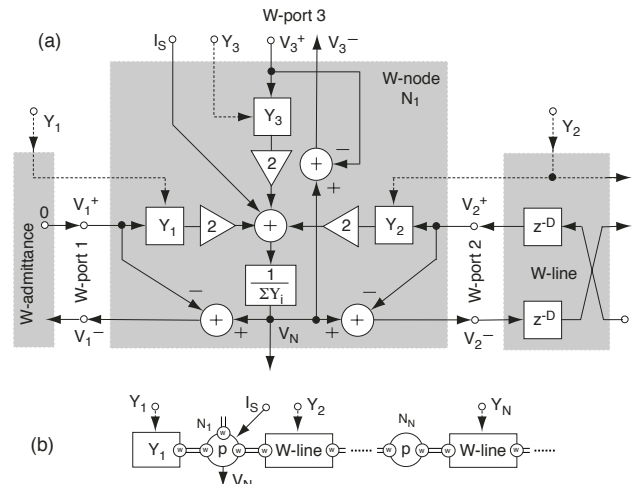


Figure 1: (a) Parallel W-node of port admittances Y_i , $i = \{1, 2, 3\}$, with associated voltage waves V_i^+ and V_i^- . Port 3 is unconnected. Current source I_s feeds the junction. (b) Symbolic notation.

where index k refers to spatial position and index n to time moment.

To build networked physical models, the continuity of physical variables must be guaranteed when connecting network components such as delay lines or lumped impedances/admittances. This is done according to Kirchhoff type of continuity laws. A network element that realizes this for wave-based models is a *scattering junction*. In this paper we discuss the formulations for the *electrical domain*, although in physical modeling of musical instruments the *acoustical* and *mechanical* domains are common. The analogy between these domains makes it easy to use a unified mathematical formalism.

For a parallel junction node (denoted by N) of K digital waveguides or lumped admittance elements, the Kirchhoff constraints are

$$\begin{aligned} V_1 &= V_2 = \dots = V_K = V_N \\ I_1 + I_2 + \dots + I_K + I_S &= 0 \\ I_i &= Y_i V_i \end{aligned} \quad (1)$$

where V_i and I_i are the total voltage and current of the i th branch¹, respectively, V_N is the common voltage of coupled branches, Y_i are admittances of the branches, and I_S is a current source feeding the junction, see Fig. 1.

When port voltages are given by incoming (+) and outgoing (-) wave components $V_i = V_i^+ + V_i^-$, and admittances Y_i attached to each port by $Y_i = I_i/V_i$, the junction voltage V_N and scattered voltage waves V_i^- can be obtained as:

¹Note that capital letters denote transform variables. For instance, V_i is the z-transform of the signal $v_i(n)$.

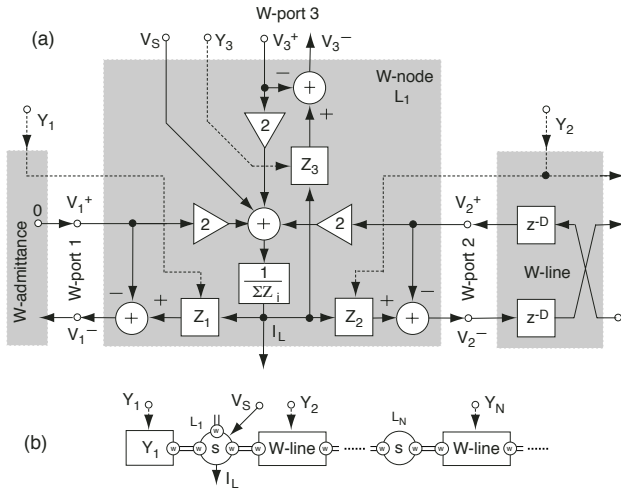


Figure 2: (a) Series W-node (loop) of port admittances $Y_i = 1/Z_i$, $i = \{1, 2, 3\}$, with associated voltage waves V_i^+ and V_i^- . Port 3 is unconnected. Current source I_S feeds the junction. (b) Symbolic notation.

$$V_N = \frac{1}{Y_{\text{tot}}} \left(I_S + 2 \sum_{i=1}^K Y_i V_i^+ \right) \quad (2)$$

$$V_i^- = V_N - V_i^+ \quad (3)$$

where $Y_{\text{tot}} = \sum_{i=1}^K Y_i$ is the sum of all admittances to the junction. The resulting junction, a parallel W-node (wave node), is depicted as a DSP structure in Fig. 1. A symbolic notation used in this study is also shown. The delay lines or termination admittances are connected to the W-ports of a W-node.

For a series connection of port admittances², i.e., a series W-node (denoted by L) of M ports, the Kirchhoff rules are written as

$$\begin{aligned} I_1 = I_2 = \dots = I_M = I_L \\ V_1 + V_2 + \dots + V_M + V_S = 0 \\ I_i = Y_i V_i \end{aligned} \quad (4)$$

where I_L loop current common to all ports. This results in voltage wave equations

$$I_L = \frac{1}{Z_{\text{tot}}} \left(V_S + 2 \sum_{i=1}^M V_i^+ \right) \quad (5)$$

$$V_i^- = Z_i I_L - V_i^+ \quad (6)$$

where voltage wave components at ports are as in Eq. 2, and impedances are $Z_i = 1/Y_i$ and $Z_{\text{tot}} = \sum_{i=1}^M Z_i$. Figure 2(a) depicts a DSP structure for computing the series connection, and Fig. 2(b) is its symbolic notation used in this study.

2.1 Termination of W-nodes

The DWG node formulations shown in Figs. 1 and 2 above can realize any discrete-time LTI parallel or series connections of arbitrary admittances Y_i . They must be positive real to guarantee passivity. If the admittances are real-valued (frequency-independent), the nodes are memoryless, and the computation can be optimized for a minimum number of operations such as multiplications.

While direct realization of arbitrary admittances in the formulations above looks convenient, it is often desirable to keep the nodes themselves memoryless. In order to realize arbitrary admittances with real-valued coefficients Y_i (or Z_i), we have to modify the structures. Figure 3 depicts the case of a parallel node with feedback of V^- to V^+ through filter $H(z)$.

²An impedance analog type of formulation for a series connection, with current waves at ports, results in the same structure as the parallel node of admittances in Fig. 1.

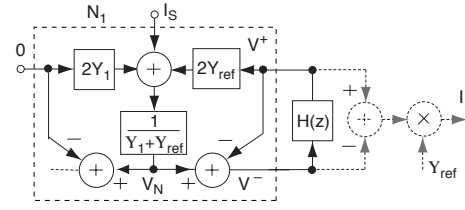


Figure 3: A network for the derivation of admittance realizations with real-valued coefficients Y_i for a parallel connection.

For generality we may assume that Y_1 and I_S in Fig. 3 form a Norton's equivalent of an arbitrary DWG network reduced to a single admittance $Y_1(z)$ and current source $I_S(z)$ for a parallel connection. Instead of an arbitrary admittance for the port to the right we attach a real-valued reference admittance Y_{ref} and a feedback of the outgoing wave $V^-(z)$ through transfer function $H(z)$ back to the incoming wave terminal. Now we can write

$$V_N(z) = (I_S(z) + 2H(z)V^-(z)Y_{\text{ref}})/(Y_1(z) + Y_{\text{ref}}) \quad (7a)$$

$$V^-(z) = V_N(z) - H(z)V^-(z) \quad (7b)$$

By eliminating V^- and solving for $V_N(z)$ we get

$$V_N(z) = \frac{I_S(z)}{Y_1(z) + \frac{1-H(z)}{1+H(z)}Y_{\text{ref}}} \quad (8)$$

which shows that the reference admittance Y_{ref} together with feedback through $H(z)$ corresponds to admittance

$$Y(z) = \frac{1-H(z)}{1+H(z)}Y_{\text{ref}} \quad (9)$$

in the formulation of a DWG port without feedback (as for Y_1 in Fig. 3). For the dashed line part $\{V^+(z) - V^-(z)\}Y_{\text{ref}}(z) = Y(z)V_N(z) = I(z)$, i.e., the current through $Y(z)$.

Let's now investigate different choices of selecting $H(z)$. The simplest case is when $H(z) = 0$, which is a resistive termination at a port of a node, and it does not deviate from the standard DWG formalism presented before. Notice that this is also compatible with the Wave Digital Filter conductance/resistance formulation [5], for which $Y_R = 1/R = Y_{\text{ref}}$.

From Fig. 3 we can easily see that the delay-free component of $H(z)$ must be equal to zero, otherwise the feedback loop created is (in a general case) not computable.

Next we try the case $H(z) = z^{-1}$, i.e., with a feedback through a unit delay. For that case

$$Y_C(z) = \frac{1-z^{-1}}{1+z^{-1}}Y_{\text{ref}} \quad (10)$$

Figure 4, curve C, characterizes the admittance of $Y_C(z)$, which at low frequencies ($f \ll 1/2T_s$) resembles an analog capacitor with capacitance value

$$C = T_s Y_{\text{ref}}/2 \quad (11)$$

Here T_s is the sampling period applied. This corresponds to the WDF capacitance formulation [5]. When $H(z) = -z^{-1}$ the admittance realized will be

$$Y_L(z) = \frac{1+z^{-1}}{1-z^{-1}}Y_{\text{ref}} \quad (12)$$

Figure 4, curve L, characterizes the admittance of $Y_L(z)$. At low frequencies it now resembles an analog inductor of

$$L = T_s/(2Y_{\text{ref}}) \quad (13)$$

This corresponds to the WDF inductance formulation [5]. For $H(z) = gz^{-1}$, parameter g varying $-1 \dots 0 \dots 1$, the admittance obtained varies from inductive (lossless) to resistive to capacitive (lossless) as characterized in Figs. 4.

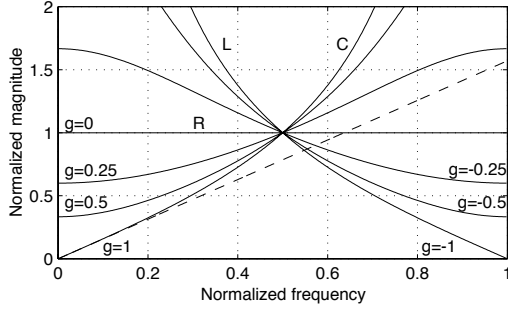


Figure 4: Normalized admittance $|Y/Y_{\text{ref}}|$ for WDF elements with delay feedback coefficient $g = -1 \dots 1$. Frequency scale normalized to Nyquist frequency. Specific cases: L = inductance, C = capacitance, R = resistance. Admittance of an analog capacitance, approximated by the WDF capacitance, is plotted by dashed line.

A useful property of mapping Eqs. (9) is that allpass forms admittances are mapped to allpass forms, i.e., it is easy to realize lossless admittances and to guarantee stability and numerical robustness of models. Notice however that due to the bilinear mappings in Eqs. (10) and (12) the capacitors and inductors realized do not show a good match with the equivalent analog components at frequencies approaching the Nyquist frequency (see admittance of curve C in Fig. 4. Only on a warped angular frequency scale Ω ,

$$\Omega = (2/T_s) \tan(\omega T_s/2) \quad (14)$$

the admittances of the digital capacitance and inductance of Eqs. (10) and (12) match with their analog counterparts [5]. This is not always a problem, because often a good match at low frequencies is enough, or it is possible to design pre-warped frequency responses such that the final realization has a desired frequency behavior. Another choice is to approximate capacitors and inductors with higher-order expressions either in the DWG formulation of Figs. 1 and 2 or by higher-order $H(z)$ filters in Figs. 3 and 5.

Higher-order filters $H(z)$ are useful also for realizing more complicated system components than the basic lumped elements, such as complex resonators, that are common in musical instruments. The bridge admittance of the guitar is an example thereof [1].

2.2 Kirchhoff Digital Filter (KDF) formulation

An alternative formulation to realize port admittances is shown in Fig. 5(a). Now we can write

$$V(z) = (I_S(z) - H(z)V(z)Y_x)/(Y_1(z) + Y_x) \quad (15)$$

By solving for $V(z)$ we get

$$V(z) = \frac{I_S(z)}{Y_1(z) + (1 + H(z))Y_x} \quad (16)$$

which shows that feedback through coefficient Y_x and $-H(z)$ corresponds to admittance

$$Y(z) = (1 + H(z))Y_x \quad (17)$$

In order to realize an arbitrary admittance $Y(z)$ we need to set

$$H(z) = \frac{Y(z)}{Y_x} - 1 \quad (18)$$

By selecting Y_x to be equal to the zero-delay component $y(0)$ in the impulse-response of $Y(z)$, filter $H(z)$ will include a delay and the DSP structure is computable. It is easy to find that any (delay-free) $Y(z)$ of FIR or IIR form can be realized in this way. For the dashed line part in Fig. 5 we can derive

$$I(z) = A(z) - B(z) = Y(z)V(z) \quad (19)$$

i.e., it represents the current in $Y(z)$. In this paper we call the structure the Kirchhoff Digital Filter (KDF) solution because both Kirchhoff variables $V(z)$ and $I(z)$ related to $Y(z)$ are explicitly available

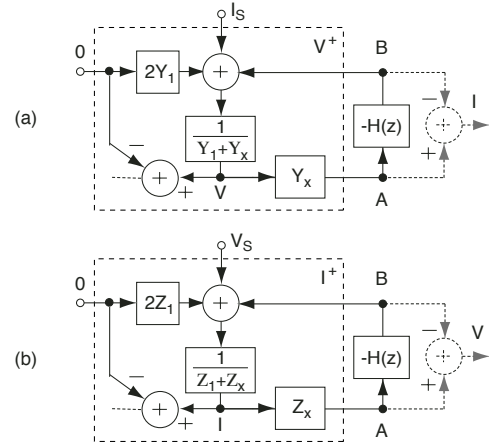


Figure 5: (a) Parallel and (b) series realization of a lumped component (right-hand side) by a method that is called here the Kirchhoff Digital Filter (KDF) formulation.

in the structure. Any number of lumped elements $Y(z)$ can be connected in parallel in this way, and this is compatible with the wave-based components as shown by the left-hand side in Fig. 5(a). A KDF-type series connection is depicted in Fig. 5(b).

For a resistive admittance $Y = 1/R$ and $Y_x = Y$ in Fig. 5(a) we get $H(z) = 0$, i.e., there is again no feedback and $I(z) = V_N(z)/R$. For an analog capacitor we may use different KDF approximations, but the best lossless approximation is equivalent to the WDF capacitor, i.e., $Y(z) = \{(1 - z^{-1})/(1 + z^{-1})\}Y_{\text{ref}}$ and $Y_x = Y_{\text{ref}}$, which yields

$$H_C(z) = \frac{-2z^{-1}}{1 + z^{-1}} \quad (20)$$

A KDF inductor, equivalent to a WDF inductor, can be formulated in a similar way. Notice that for KDFs there is no such restriction that was stated for WDFs by equation (9).

3. GENERAL NETWORK STRUCTURES

The parallel and serial connections (they are called adaptors in WDFs), as derived above, are examples of complete networks connected through a single node. In a general case of DWGs there is need to construct circuits and networks where parallel and serial substructures are connected to constitute more complex parallel and series structures. The goals are (a) generality for any physically meaningful structures, (b) computational efficiency, (c) localized effect of block parameters, and (d) scheduling of computation operations so that delay-free loops are avoided³. We have developed and applied the BlockCompiler (BC) [9] software environment to experiment with different modeling paradigms separately and mixing the paradigms in a single model.

There are different strategies of network computation towards the goals above, but it seems that tree-structuring of scheduling is a useful common feature. We will present below a method that is conceptually based on the Thévenin's and Norton's methods [10]. A given network structure is composed into a tree structure so that computation starts from leaves, propagating towards the root by mapping substructures to Thévenin and Norton equivalents until the root block is reached. There the full state of its variables can be computed. This will then propagate back towards leaves, giving the full state of the variables in each block until all blocks are finished for that sample period. This resembles the strategy in the Binary Connection Tree (BCT) method proposed in [11].

³Computability is no problem when parallel and series connection blocks are separated by delay lines as in Figs. 1(b) and 2(b), but for lumped element connections strict rules must be followed.

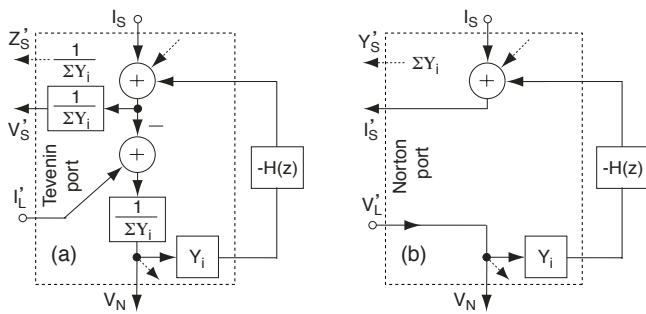


Figure 6: Formulation of a parallel connection as (a) Thevenin equivalent and (b) Norton equivalent for KDF admittances. This can be modified according to Fig. 3 for WDF admittances.

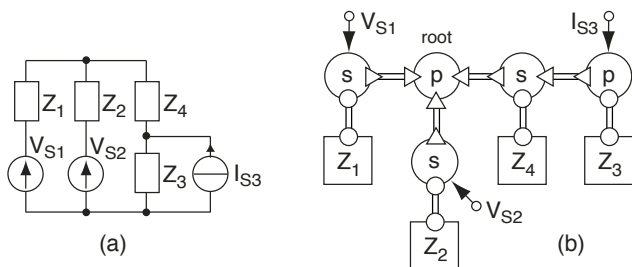


Figure 7: Example of (a) an electric network as (b) a connection tree composed of series and parallel connections following the notations introduced in Figs. 1 and 2. Thevenin and Norton ports are denoted in (b) by triangles.

Figure 6(a) shows how a parallel KDF connection is converted into a Thevenin equivalent. The Thevenin port acts as a voltage source V_S' and impedance $Z_S' = 1 / \sum Y_i$ that can feed a series connection to the left. When the node current I_L' of that series connection block is known, it is fed back to the parallel connection node in order to compute its voltage V_N . Figure 6(b) shows the conversion of a parallel KDF node into a Norton equivalent to be connected as a source to another parallel node on the left-hand side. The formulation of a series KDF connection into a Thevenin and a Norton equivalent is developed in a similar way. When WDF components are used, the feedback parts have to be made according to the principle in Fig. 3.

Figure 7 depicts an electric circuit example of combining series and parallel connections of impedances and sources. The structure can be specified for example by syntax:

```
par (ser (vs1, z1), ser (vs2, z2), ser (z4, par (is3, z3)))
```

where functions `par` and `ser` correspond to parallel and serial connections, respectively. The circuit can be represented as a tree in numerous ways. The selection of the root node is particularly important when attaching nonlinear elements [11] because the root is the only connection node where the relation of voltages and currents can be computed explicitly in a single pass.

4. DISCUSSION AND CONCLUSIONS

This paper links tightly together different approaches to physics-based modeling by DSP as well as general circuit and network simulations in the discrete-time domain. After discussing the Digital Waveguide (DWG) principles the basic Wave Digital Filter components are shown as a variation of the way to compute lumped admittances/impedances. The close relation of DWGs and WDFs is well known [6], but the approach taken in this paper broadens the view and methodology of physical modeling beyond basic elements and structures as well as filter design beyond traditional filter types to meet the requirements of complex physical systems.

The paper introduces also a further variant to realize lumped admittances/impedances. Because the variables used are explicit Kirchhoff variables, the realizations are called here the Kirchhoff Digital Filters (KDF). It is evident that the WDF and KDF approaches are compatible. Both of them have the advantage that the "scattering part" of computation is memoryless.

As a final development of this paper the combination of parallel and series connections into more complex (parallel and series) connections is investigated. An approach to organize a circuit or a network as a tree-structure for two-pass computation of the nodes is proposed, based on using the Thevenin's and Norton's methods for equivalent circuit ports. This is applicable to both the WDF and the KDF structures.

At the same time of formulating ways to simulate physical systems in the discrete-time domain, this study opens many new questions that were only briefly mentioned or not touched at all in this paper. Among such topics are higher-order admittance elements and their design, realizations for elements such as transformers, gyrators, controlled sources, etc. Future tasks include also a systematic comparison of the approaches from the viewpoints of efficiency, numerical robustness, other possible limitations of each approach, their applicability to modeling non-LTI systems, as well as their relations to other methods such as FDTD schemes and modal decomposition techniques.

One of the main motivations of the study has been to develop flexible and efficient software tools for multi-paradigm modeling of acoustic systems, particularly of musical instruments. The work under development includes a systematic implementation of the techniques in BlockCompiler [9], a block-based tool for real-time simulation.

5. ACKNOWLEDGMENTS

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